3101
DUAL JK FLIP-FLOP
MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 3101 dual JK flip-flop is a MOS monolithic integrated circuit utilizing P-Channel enhancement technology. This device can be utilized as a logic block in an all MOS system, or as a breadboarding flip-flop in designing custom integrated circuits. Input protection is provided on all inputs.

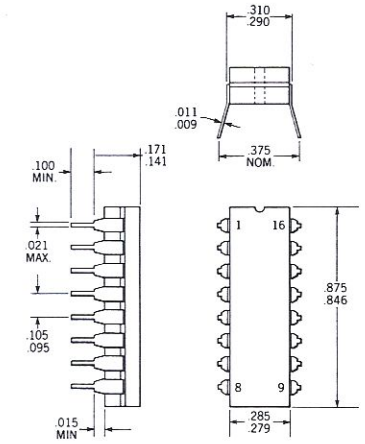
FEATURES

- **INPUT PROTECTION**
- **BUFFERED OUTPUTS**
- **ASYNCHRONOUS SET AND CLEAR**
- **SEPARATE CLOCK LINES**

ABSOLUTE MAXIMUM RATINGS (Notes 1 & 2)

Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +85°C
Power Dissipation at +25°C	200 mW
Positive Voltage on any pin	+0.3 V
Negative Voltage on any input pin	−30 V

PHYSICAL DIMENSIONS
16 Lead Dual In-Line



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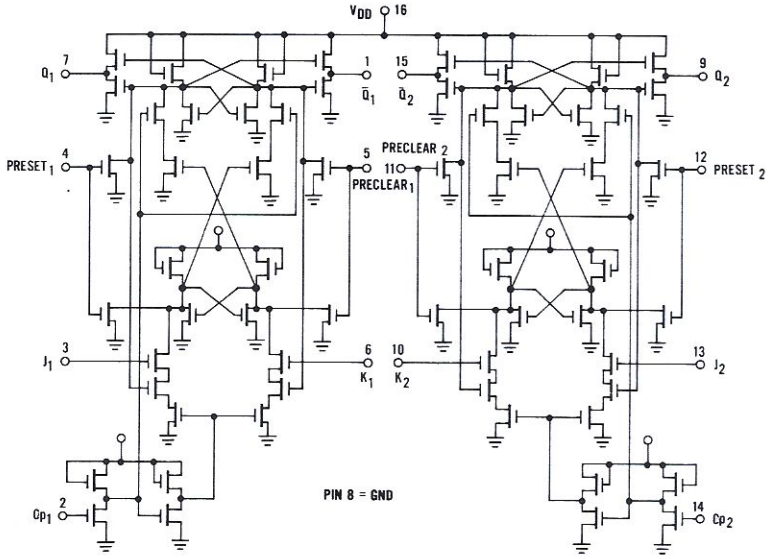
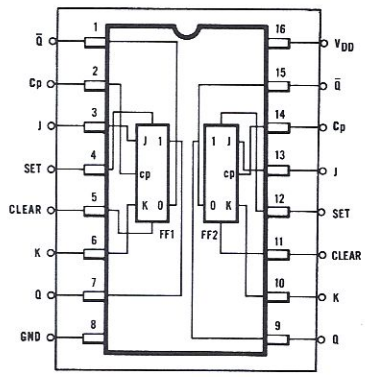
SCHEMATIC DIAGRAM



CONNECTION DIAGRAM
(TOP VIEW)



NOTE: Polarity indicators (o) external to the solid box conform to MIL-STD-806B where 0 indicates the less positive state is active. Internal to the box and in the remainder of this data sheet conventional MOS polarities are used, where HI = "1" ≃ −10V and LO = "0" ≃ Gnd.

NOTES:
(1) These ratings are limiting values above which serviceability may be impaired.
(2) Voltage levels are with respect to the GND Pin.

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ELECTRICAL CHARACTERISTICS ($V_{DD} = -27 \pm 2$ Volts, $T_A = 25°C$ unless otherwise specified)

CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
Clock Frequency	DC		250	kHz	$V_{DD} = -26$ V
Clock Amplitude	−9.0			Volts	
Clock Pulse Width	1.0			μs	
Input Leakage Current			1.0	μA	$V_{IN} = -20$ V
Input Capacitance		5.0		pF	$V_{IN} = 0$ V
Input Logic Levels					
"0" Level	0		−2.0	Volts	
"1" Level	−9.0			Volts	
Input Data Pulse Width	1.0			μs	
Output Impedance to Ground			1.0	kΩ	
Output Logic Levels					
"0" Level			−1.0	Volts	
"1" Level	−10			Volts	
t_{setup}		0.5		μs	
$t_{release}$		0.5		μs	
t_{pd+}		1.0		μs	
t_{pd-}		0.5		μs	
Power Consumption		75		mW	

TRUTH TABLE

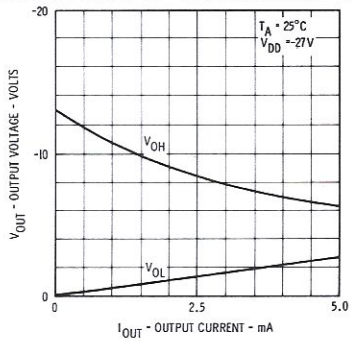
J $t = n$	K $t = n$	Q $t = n + 1$
0	0	X^n
0	1	0
1	0	1
1	1	$\overline{X}^n$

Logical '1' is more negative than −9.0 V

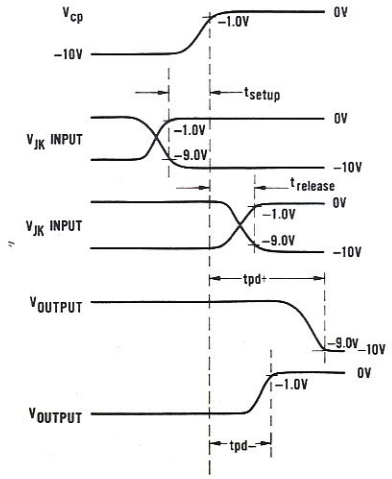
Logical '0' is more positive than −2.0 V and ≤ 0

X^n is the output state at time n

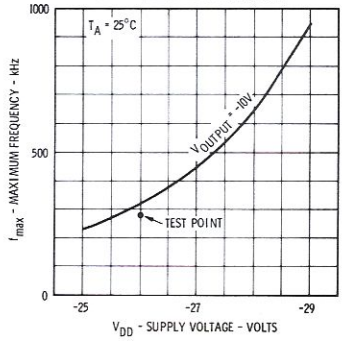
TYPICAL OUTPUT CHARACTERISTICS



TYPICAL SWITCHING WAVEFORMS



MAXIMUM FREQUENCY VERSUS SUPPLY VOLTAGE



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